with the voltage ramp, said operational amplifier operating in a linear mode, whereby said output voltage approximates a multiple of the voltage ramp;

d. transistor means electronically connected to said operational amplifier circuit, said transistor means operating in linear mode during capacitor charging, and subsequently reaching a full-ON state; and

e. energy storage load means connected to said transistor means for receiving a full power supply after said transistor means reaches its said full-ON state.

Please cancel claims 5 and 9 – 16, and add the following new claims:

8. ~~17.~~ The inrush circuit of claim 1, further comprising time delay means connected to said means for providing a voltage ramp.

9. ~~18.~~ The inrush circuit of claim ~~17~~ 8, wherein said time delay means reaches threshold in about 50 ms.

10. ~~19.~~ The inrush circuit of claim 1, wherein said energy storage load means is a bulk capacitor.